

Notice of References Cited

Application/Control No.

09/586,191

Applicant(s)/Patent Under

Reexamination

ISLES, ADRIAN J.

Examiner

Ayal I Sharon

Art Unit

2123

Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,555,199	09-1996	Cunningham et al.	703/1
	B	US-6,380,945	04-2002	MacInnis et al.	345/602
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Weems, Charles C. Jr. "CmpSci 535 Notes from Lecture 9: Memory Hierarchy and Caching". © 1996. Printed on 6/27/03 from http://www.cs.umass.edu/~weems/CmpSci535/535lecture9.html
	V	Bayoumi, M. et al. "A Look-Up Table VLSI Design Methodology for RNS Structures Used in DSP Applications." IEEE Transactions on Circuits and Systems. Vol. 34, Issue 6, June 1997. pp.604-616.
	W	Chang, Y. et al. "Cache Memory Protocols" Wiley Encyclopedia of Electrical and Electronics Engineering Online. Article Online Posting Date: Dec. 27, 1999.
	X	Patten, W.N. et al. "A Minimum Time Seek Controller for a Disk Drive." IEEE Transactions on Magnetics. Vol.31, Issue 3, May 1995. pp.2380-2387.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited

Application/Control No.

09/586,191

Applicant(s)/Patent Under
Reexamination
ISLES, ADRIAN J.

Examiner

Ayal I Sharon

Art Unit

2123

Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Grochowski, E. et al. "Issues in the Implementation of the i486 Cache and Bus." 1989 IEEE Int'l Conf. on Computer Design. (ICCD '89). Oct. 4, 1989. pp.193-198.
	V	Cong, J. et al. "FlowMap: An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Vol. 13, Issue 1, Jan.1994. pp.1-12.
	W	Parhami, B. et al. "Optimal Table Lookup Schemes for VLSI Implementation of Input/Output Conversations and Other Residue Number Operations." [Workshop on] VLSI Signal Processing, VII, 1994. Oct. 28, 1994. pp.470-481.
	X	Zukowski, C. et al. "Putting Routing Tables in Silicon", IEEE Network. Vol.6, Issue 1, Jan. 1992. pp.42-50.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.